Design of Fault Tolerant Reversible Multipliers using novel Reversible Gates

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ABSTRACT:

In recent scenario, the reversible logic design inducing more interest due to its low power consumption. For its enormous potential, it is used in quantum computing, nanotechnology, Quantum Dot Cellular Automata (QCA) and Digital Signal Processing. In reversible logic the major challenges are Fault- tolerance, quantum cost and garbage outputs. The multipliers are the heart of the computing hardware for the data manipulation. In this paper, novel fault-tolerant reversible KMD gates are proposed. The proposed gates are used to build the minimum complexity multiplier in Quantum cellular automata. Since the gates are fault tolerant, the designed multiplier also fault-tolerant. The simulation results, shows that the proposed multiplier has better improvement with respect to the existing, in terms of gate count and constant input. The entire structure was simulated in QCADesigner.

Keywords ***-- Reversible Logic, Fault Tolerant, KMD gate, Quantum Cellular Automata(QCA).***

I. INTRODUCTION:

Irreversible hardware computation results in power dissipation due to information loss. As demonstrated by R.Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss[1].According to his research, combinational logic circuits dissipate heat in an order of kTln2 joules of energy for every bit of information that is erased where k is the Boltzman constant and T is the operating temperature[1].

Information is lost when the circuit implements non bijective functions. Therefore in irreversible logic circuit the input vector cannot be recovered from its output vectors. Reversible logic circuit realizes only those functions having one-to-one mapping between its input and output assignments. Hence in reversible circuits no information is lost. According to Bennett zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design[2].

Gate leakage current, interconnection noise, design complexity and stray capacitance are most common issues faced by CMOS Technology. These problems are the drawbacks of CMOS technology[3]. QCA is a growing innovation in recent years which seems to be a good competitor for the next generation of digital systems and widely utilized as a part of advanced design works. Diminutive size, faster speed, extremely scalable feature, ultra low power consumption and better switching are most important metrics of QCA. For logic evaluation it uses location of electrons[4]. The polarization of one cell induces a polarization in a neighboring cell through the Coulomb interaction in a very non-linear fashion [7]. Recent papers show that QCA circuits can achieve high density, fast switching speed and room temperature operation [4].

II. BASICS OF REVERSIBLE LOGIC

The following characteristics should be checked for their reversibility.

They are Quantum cost, Constant inputs, Number of gates used and Garbage output.

Quantum Cost:
It refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit [3][8].

Garbage Output (G):
Unwanted output of reversible gate is called garbage output. The output of reversible gate is not used as a primary output or as input to other gates is called garbage output. Garbage outputs are needed in circuit to maintain reversibility concept [3][8].

Gate Count:
Number of reversible gates used to realize the function [3][8].

Constant Input:
To get particular output some inputs are maintain either zero or one. This type of inputs are called Constant inputs [3][8].

III. BASIC REVERSIBLE MULTIPLIER CIRCUITS

A . *Minimum Complexity Multiplier using basic reversible gates*

A typical digital multiplier inputs two binary numbers, i.e. multiplicand $X=xn\text{-}1\ldots x1x0$ and multiplier $Y=yn\text{-}1\ldots y1y0$ and outputs the product $P=P2n\text{-}1\ldots P1\ P0$, which can be written in the following form:

$$P=\sum_{i=0}^{i=n-1}\sum_{j=0}^{j=n-1}(x_i\,y_j)2^{i+j}$$

Each of the partial product terms $Pk=xiyj$ is called a summand. In general AND gates are used to produce summands in parallel and get added using an array of adders [9]. Therefore any architecture of multiplier consist of two parts: they are partial product generation module and partial product addition array. Then some optimization have been done[6].

1) Implementation of partial product generation module: An $n\times n$ multiplier requires $n\times n$ summands and consequently AND logic operations. They have realized the partial product generation module based on Toffoli gates, no extra circuit is necessary. Furthermore, because Tofolli gates have two identical inputs and outputs, their use allows broadcasting both the multiplicand bits and the multiplier bits from gate to gate. Thus reducing the number of garbage outputs as well. The only disadvantage of TG is large quantum cost[6].

2) Implementation of addition array: This can be done in many ways. In the point of minimum complexity, the structure have contained eight full adders and four half adders. The half adder (HA) has two inputs and 2 outputs, while a full adder (FA) has 3 inputs and two outputs[6].

To implement reversible HA, they have used a single Peres gate (PG) with a constant zero on its third input and single garbage output. To implement the reversible FA, they have used HNG gate which was specially developed for full adder operation. HNG gate had 4 inputs as well as 4 outputs to maintain reversibility. The circuit includes 12 gates, 12 constant inputs, 20 garbage outputs and has the quantum cost of 64[6].

IV. KMD GATES

Basic components of multiplier is and gate, half adder and full adder. It will be designed by using KMD gate 1,2,3 as shown in Fig 1,2,3. The and gate, half adder , full adder is designed using these fault tolerant Reversible gates as shown in Fig 4,5,6.

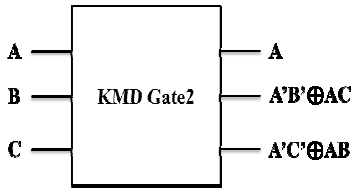

Fig .1.KMD Gate 2

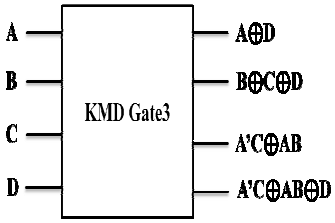

Fig.2.KMD Gate3

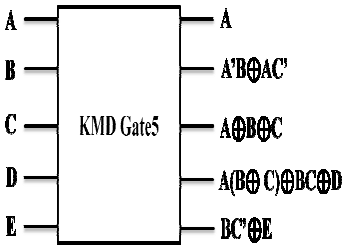

Fig.3.KMD Gate 5

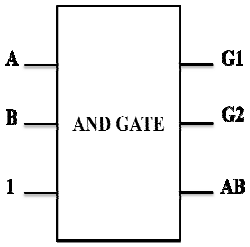

Fig .4.AND Gate using KMD 2

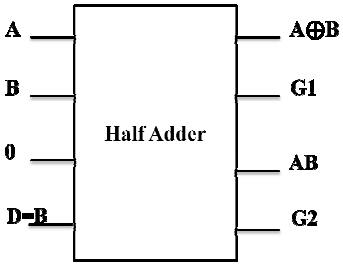

Fig.5.Half Adder using KMD 3

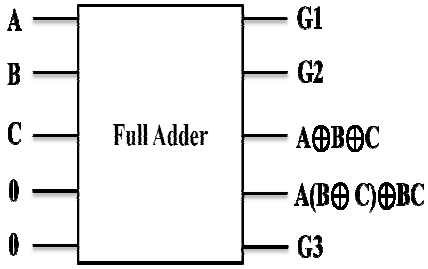

Fig.6.Full Adder using KMD 5

VII. PROPOSED REVERSIBLE MULTIPLIER USING KMD GATES

This paper proposes the fault tolerant reversible minimum complexity multiplier using reversible fault tolerant KMD gates . The partial product generation circuit and the addition array circuit are shown in Fig 7,8 respectively.

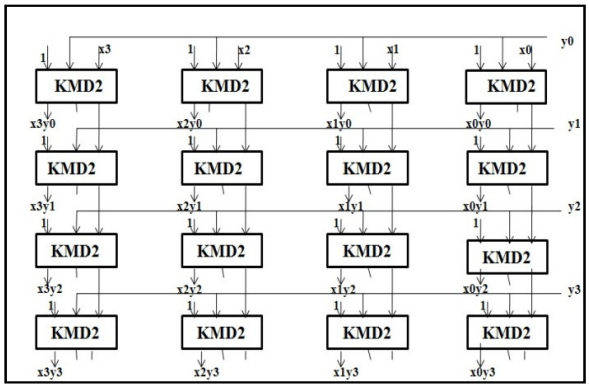

Fig .7.Proposed fault tolerant reversible minimum complexity paritial product generation circuit

The design of fault tolerant reversible partial product generation circuit composes of sixteen Reversible structures. The design constitutes of sixteen KMD 2 gates.

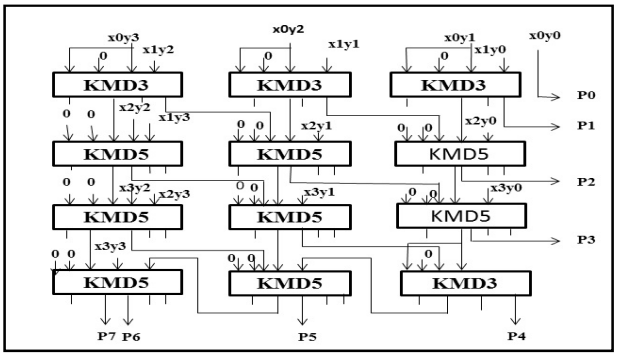

Fig .8.Proposed fault tolerant reversible minimum complexity addition array

The design of fault tolerant reversible addition array circuit composes of twelve Reversible structures. The design constitutes four KMD 3gates, eight KMD 5 gates.

VII. SIMULATION AND RESULTS IN QCA ENVIRONMENT

All the design of basic reversible logic gates was verified by using QCA Designer tool ver.2.0.3. In the bistable approximation, we use the following parameters, which are default parameters in QCA designer tool: number of samples(12800),convergence tolerance (0.001000), radius of effect(65.00nm), relative permittivity (12.900000),clock high(9.800000e-022), clock low (3.800000e-023),clock shift(0.000000e+000),clock amplitude factor (2.000000), layer separation (11.500000), maximum iterations per sample (100). In our QCA layouts, we have the goal of workable design with

compact layout. The simulation results of reversible logic gates and multipliers are shown below:

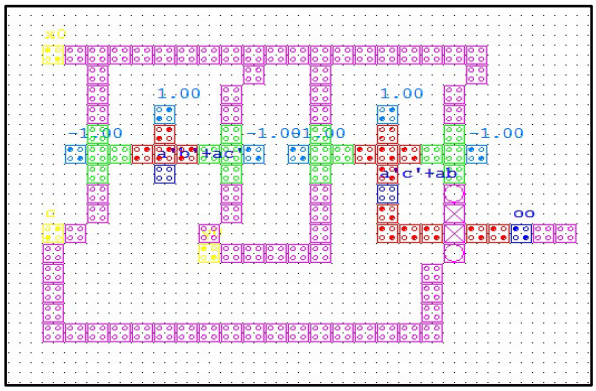

Fig .9. QCA Layout of KMD Gate 1

Quantum cost of KMD 2 is 5. The number of cells required to implement this structure is 119.

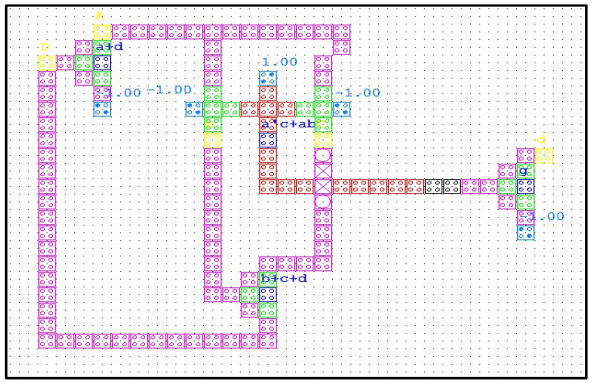

Fig .10.QCA Layout of KMD Gate 3

Quantum cost of KMD 3 is 9. The number of cells required to implement this structure is 132.

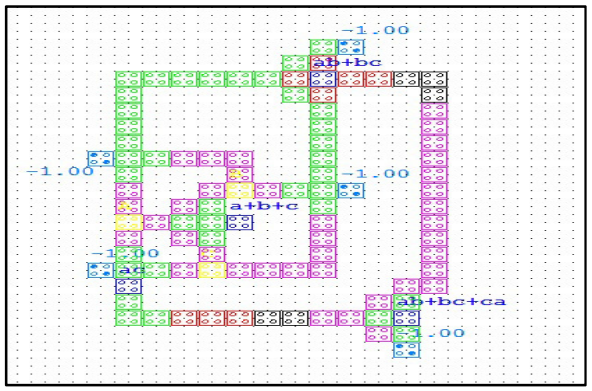

Fig .11.QCA Layout of KMD Gate 5

Quantum cost of KMD 5 is 24. The number of cells required to implement this structure is 100.

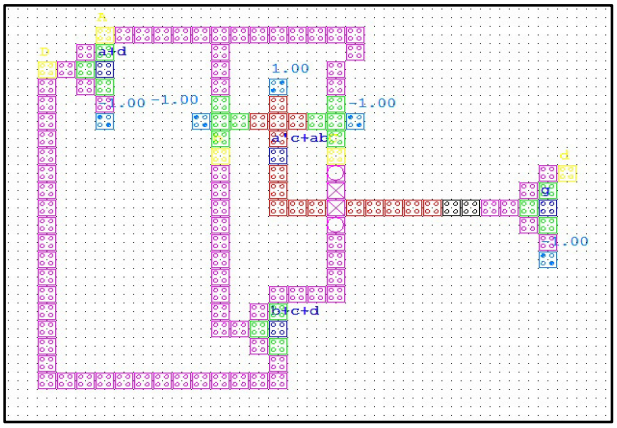

Fig .12.QCA Layout of Half Adder

Half adder constructed from KMD 3 by making C as 0 and D as B as per Fig .4.

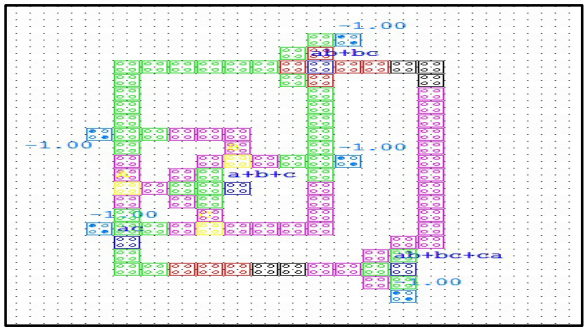

Fig .13. QCA Layout of Full Adder

Full Adder constructed from KMD 5 by making D and E as 0.

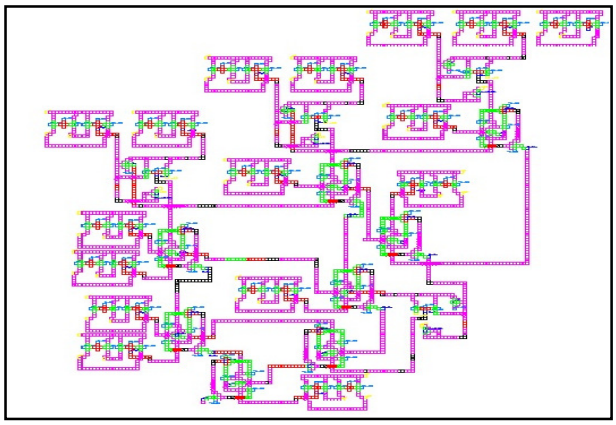

Fig .14.QCA Layout of fault tolerant reversible minimum complexity multiplier

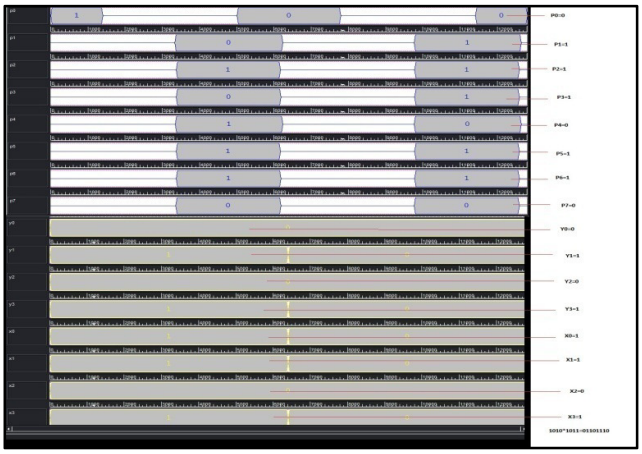

Fig .15.Output of fault tolerant reversible minimum complexity multiplier

TABLE .1. COMPARISION BETWEEN PROPOSED MULTIPLIER WITH EXISTING

Parameters	Existing [6]	Proposed
Gate Count	**36**	**28**
Constant Inputs	**40**	**36**
Quantum Cost	140	388
Garbage Output	40	64

TABLE 1 represents the comparison of proposed reversible multiplier with existing multiplier. The comparison is made between the design perspectives of gate count, constant inputs, quantum cost and garbage output.

X. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. The focus of this paper is to reduce the number of gates and constant inputs. Reversible Logic is a technology that offers less power dissipation and less heat dissipation. Using KMD gate 2, KMD gate 3 & KMD gate 5 the AND gate, half adder & full adder had been designed. The multiplication operation is performed by above mentioned blocks. The simulation result shows that improvement in Gate Count, Constant Inputs when compared with existing designs. Here, a fault tolerant reversible multiplier circuit having lowest gate complexity has been designed and achieved better performance through KMD gates.

XI. REFERENCE

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