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RESEARCH ARTICLE OPEN ACCESS

A Novel Multilevel Inverter Topology for Renewable Energy Based Distributed Power Generation

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Abstract:

This Paper proposes a multi-level inverter topology for renewable energy source based distributed power generation. It consists of isolated DC sources alternately connected in opposite polarities through power switches with antiparallel diodes. In the proposed multi-level inverter, reduced number of power switches is used when compared to the classical topologies, which results in reduction in converter cost, switching losses filter requirements, etc. The main objectives of this paper is to improve the efficiency of the multilevel inverter, and to reduce the total harmonic distortion to the possible extend. Since it produces almost pure sinusoidal output it is suitable for industrial applications operated from a n number of individual dc module. The concept of the proposed topology is explained with the assistance of a single-phase eleven-level inverter. An exhaustive comparison of the proposed topology against the classical topology is explained and hardware prototype's results are also presented. The performance of the proposed topology is tested as a single phase VSI as well as three phase VSI under MATLAB/Simulink environment.

Keywords **— Multi-Level Inverter, FFT Analysis, MATLAB/Simulink**

I. INTRODUCTION

Nowadays increasing power demand is the greatest issues on the power system demand due to rise in population and urbanization In order to compensate this the power generation are also increased. But the major drawback in convention centralized power generation system is its scale of investment for plant capacity development and mostly they are non-renewable in nature. We cannot fully depend upon the Non-Renewable energy source; we have to switch over for renewable energy sources. Almost the renewable energy sources are DC source. This kind of renewable energy sources plays a major role in Micro grid technology. Micro Grid is nothing but a cluster of more than one Renewable energy source whose capacity will not exceed 50MVA and supplies to individual load or to group of loads. To covert the DC power from Renewable energy source into AC we prefer Power inverters. The voltage stress across the switches in conventional H bridge topology is high. So we prefer multilevel inverters.There are many multilevel topology are available namely Cascade H-bridge (CHB) inverter, flying capacitor inverter (FC), Neutral point clamped converter (NPC) etc... The main disadvantages of the multilevel inverter are large number of switches and parallel capacitor for balancing the voltage. These conventional topologies need more component according to increase in number of levels in output voltage. So, researchers are working to reduce the components count for given number of voltage levels. Various ideas are approached by the researchers to reduces the count of the component, they are

i) Topology modification of components.
ii) Employing the asymmetric source configuration or asymmetric ratio of the capacitor voltages.
iii) By combing above two ideas.

This proposed topology recognizes an alternative of two level voltage sources inverter specially made for the higher voltage applications and industries usage. Using this multilevel topology, the amplitude of the output voltage will be increased or decreased based on our application.Due to usage of n number of isolated DC sources the voltage stress across the switch get reduced. The three phase VSI is obtained by connecting three individual single phase VSI in star connection.

It is important to mention here that the scope of this paper is limited to introduce the topology in terms of structure, modeling, validation and comparison with other topologies. Some of other important issues that can be explored in further studies are: fault-tolerant operation for specific applications (e.g. AC drives), load sharing among input sources, switching optimization, assembly steps, reliability calculations and so on. Here we projected only the performance of the topology as single phase VSI and three phase VSI

II. PROPOSED TOPOLOGY

A. *Structure of proposed topology*

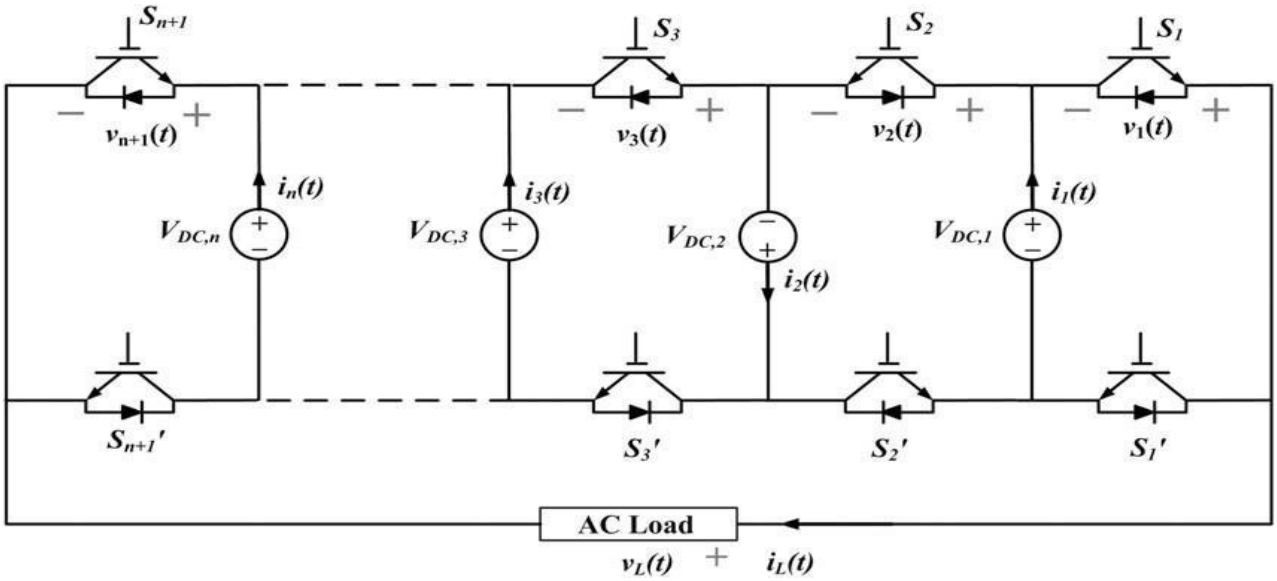


Fig1. Single phase structure of proposed topology

The single-phase proposed topology generalized structure is shown in Fig1. It consists of 'n' numbers of isolated DC source connected in series designated as, V_{DCj} {j =1 to n}, through power switches (n+1). These power switches are illustrated in Fig. 1 as insulated gate bipolar transistors (IGBTs) with anti-parallel diodes and the power switches designated as (S_j, S_j'){j =1 to n + 1}. The isolated DC sources are connected that higher terminal is connected lower potential terminal of the succeeding side of the source through power switches and vice-versa. The nodal voltages are indicated as Vj(t){j =1 to n+1} and source currents are designated as Ij(t) {j= 1 to n}. The converter feeds an AC load with V_L(t) and IL(t) respectively. This new topology divided into three parts mainly they are,

PART 1: The rightmost complimentary consists of power switches of S1 and S1' connected in series.

PART 2: The Isolated DC sources are connected in series with power switches. The level of inverter is determined number of DC source.

PART 3: The leftmost complimentary switches of S_{n+1} and S'_{n+1}. It varies according to the level of the inverter.

B. *Topology of Eleven level multilevel inverter*

In this section, the structure of proposed topology described with the help of single phase ELEVEN level inverter. It consists of five isolated dc voltage sources, which is connected alternatively. VDC1, VDC2, VDC3, VDC4, and V_{DC5} are the isolated dc sources which are connected as shown in Fig.2. There are six pairs of active power switches (S_j, S'_j) {j = 1, 2, 3, 4, 5, 6}. Each isolated DC sources consists of 66.5V to give 230V AC as an output. The above shown Circuit has 11 operating states. The respective switches are ON according to the lookup table to obtain the particular voltage level. The gate pulse is given to the IGBT switches as per the lookup table.Here, eleven level inverter is explained with Resistance. **Multiple Carrier Sinusoidal Pulse Width modulation** (SPWM) is a technique to the control the output Voltage in a converter. It is superior to other convention system there is PWM. The objective of these control scheme is to eliminate the particular dominate order of harmonics in output waveform. It is achieved by following block diagram and the look up table for Eleven level inverter is shown in Tab1.

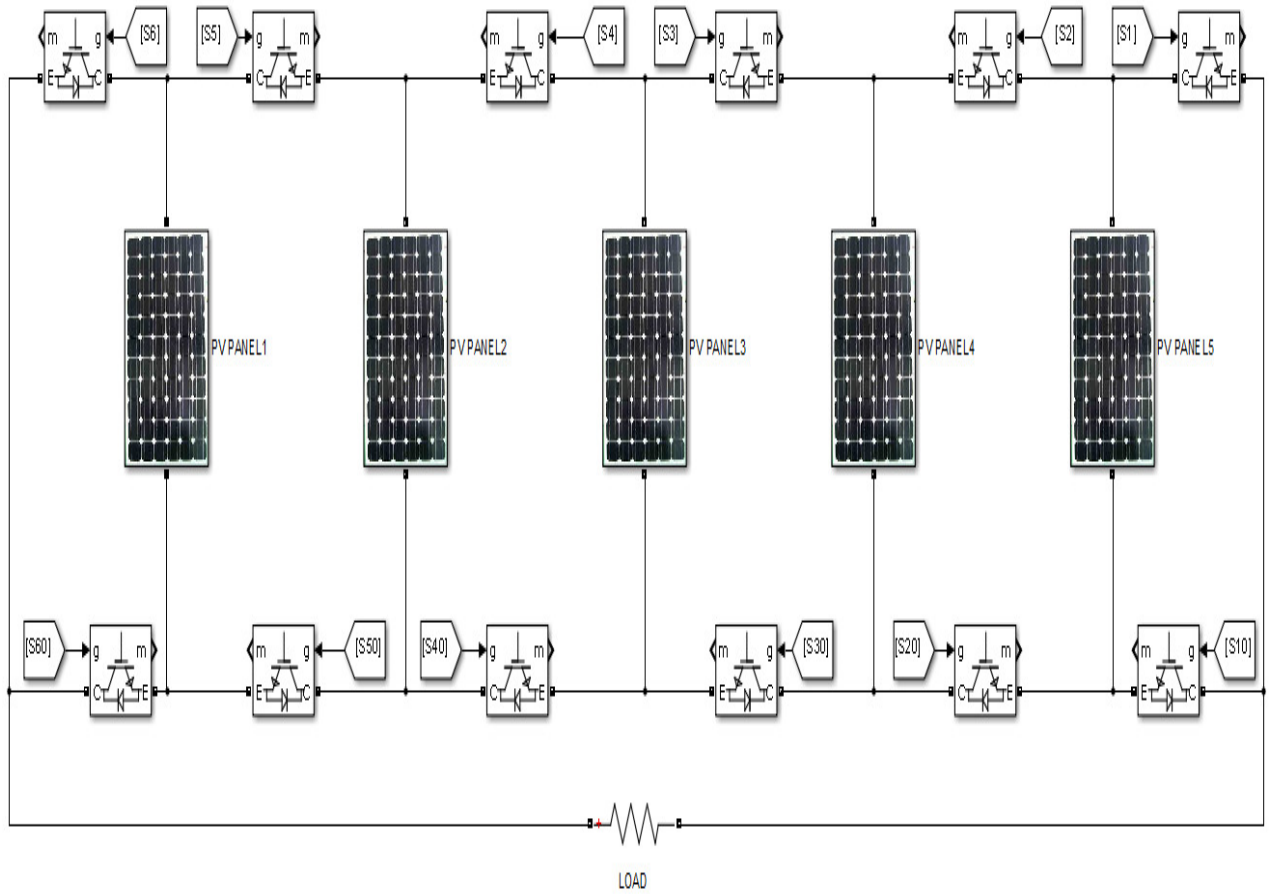
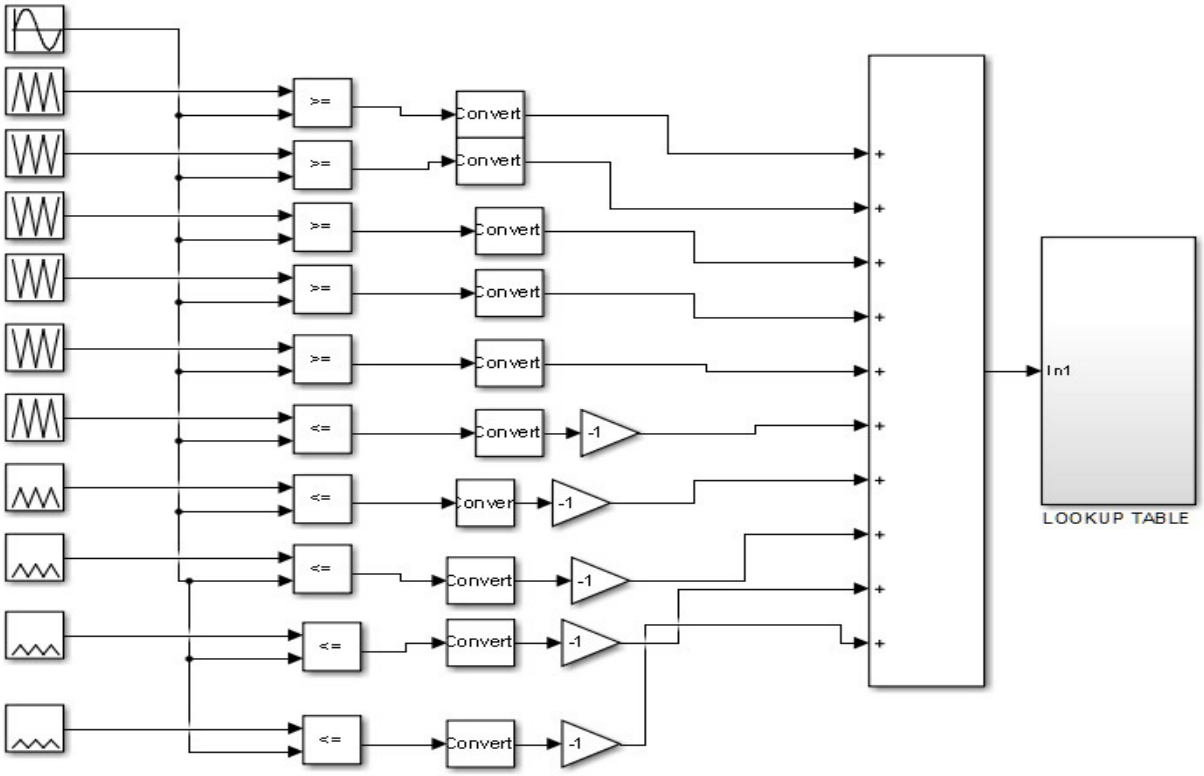


Fig2a. Single phase eleven level multilevel inverter



Tab1. Lookup table

III. SIMULATION RESULTS

A. Control scheme

In these proposed system, the Multiple Carrier Sinusoidal Pulse Width Modulation is preferred to reduce the harmonic content in the output voltage. In these technique 50Hz reference waveform is compared with 10 kHz reference waveform. So, it is projected as in following **Fig.4**.

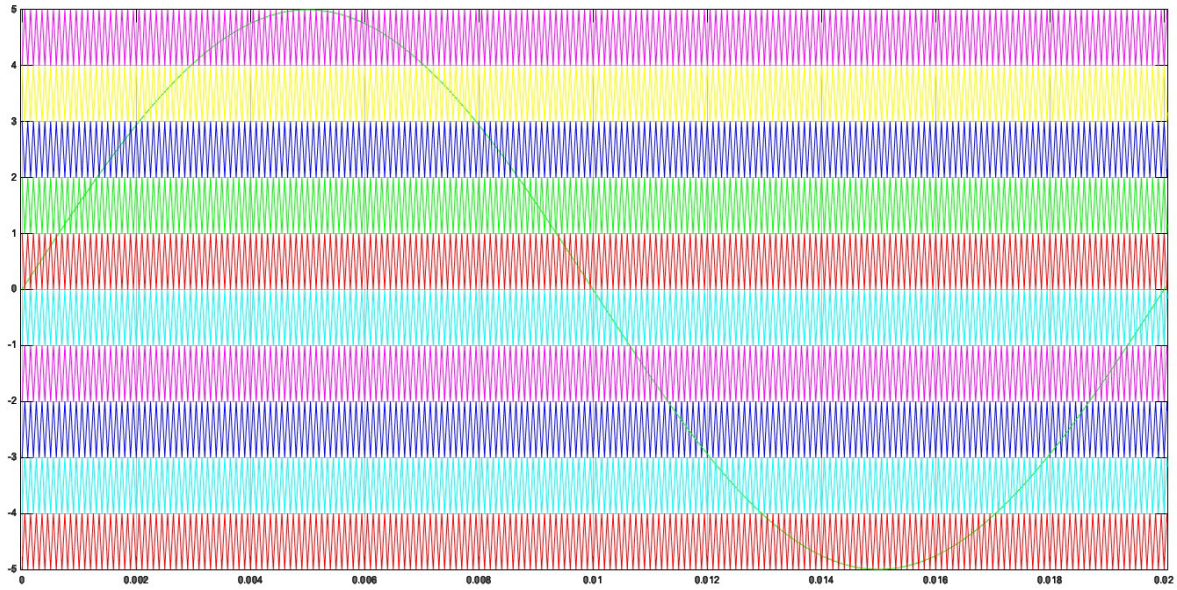


Fig4. Reference and carrier waveform

Due to this sinusoidal pulse width modulation in this proposed system Total Harmonic Distortion (THD) level in output voltage is reduced to **13.58%** which is projected in following **Fig.5.**

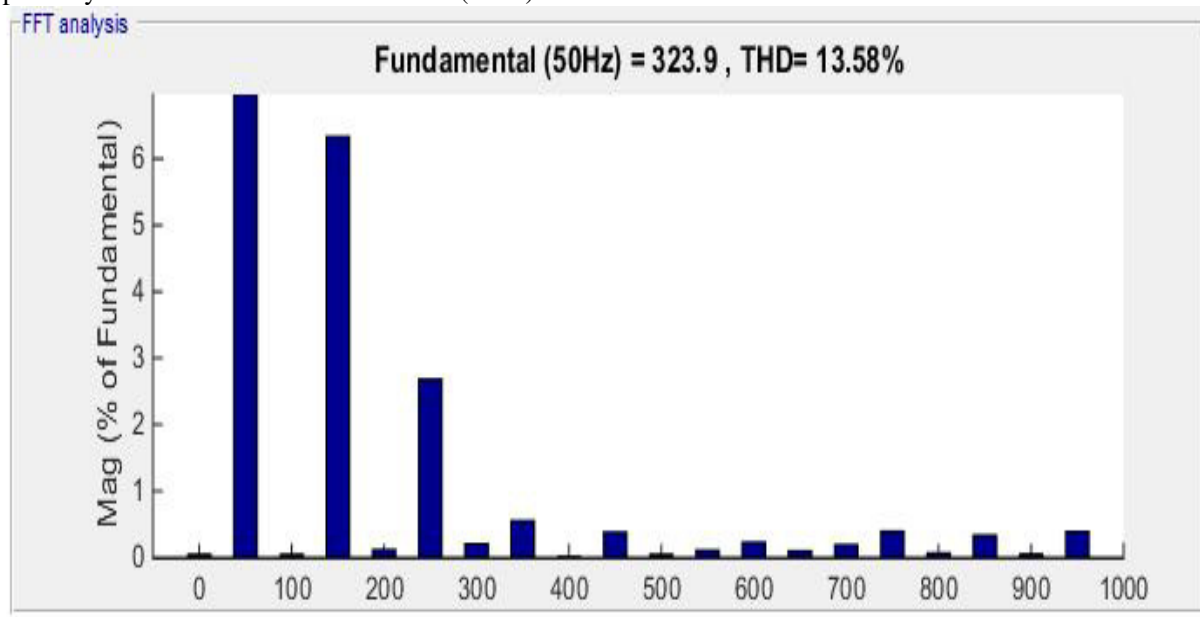


Fig5.THD Analysis of output waveform

As a result of this control scheme output voltage of proposed topology is looking like a sinusoidal waveform. It is because high resolution split up of reference waveform. The resolution, steps or number of level in the output voltage waveform is directly proportional to number of split ups or number of triangular wave used as carrier waveform. It is inferred in **Fig6.**

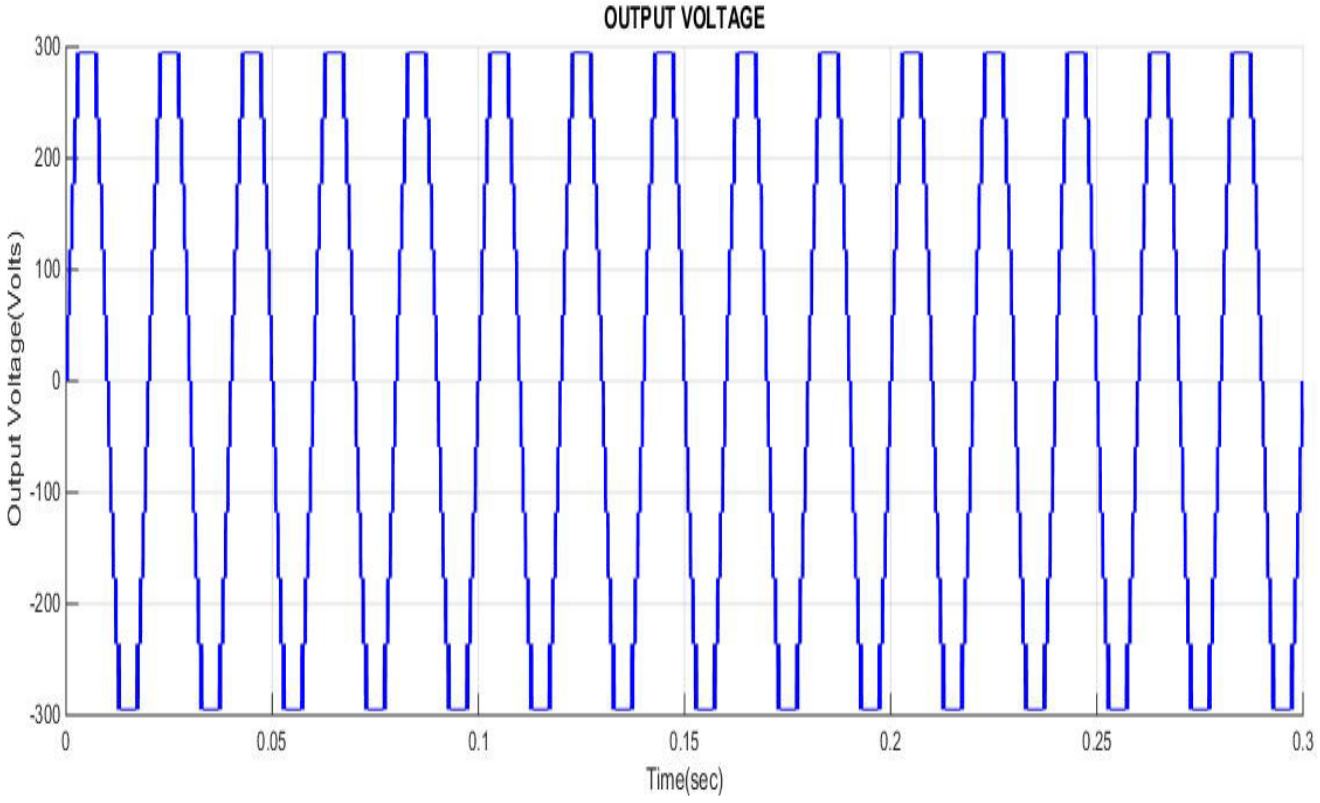


Fig6. Output voltage waveform of proposed system at single phase setup

B. B. Performance of proposed topolgy under three phase setup

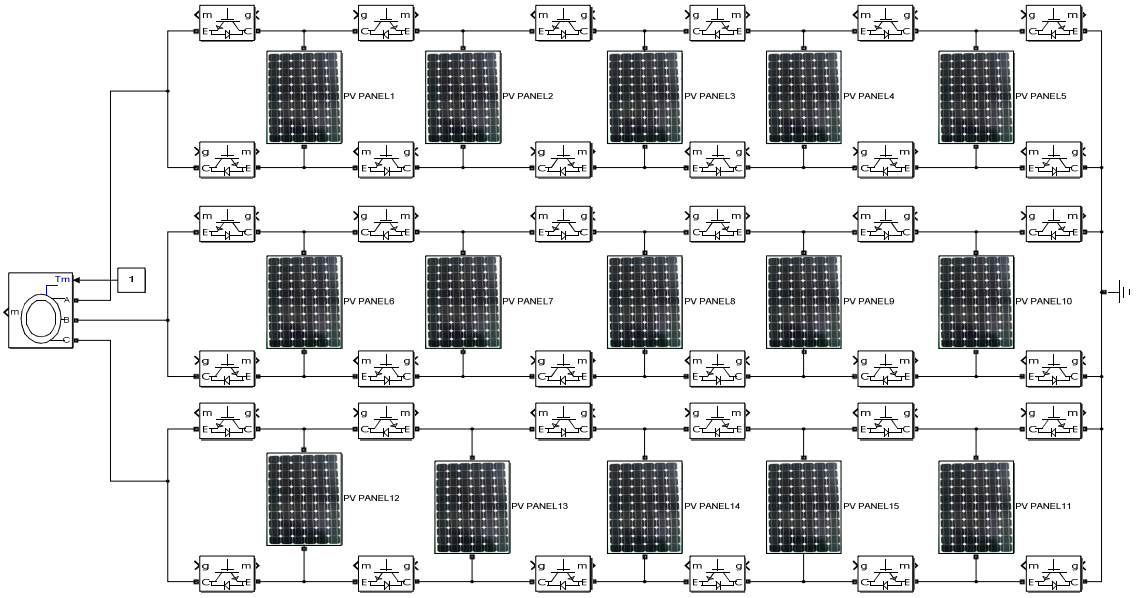


Fig7. Simplified Circuit Diagram of Proposed Three phase Topology

The performance of the proposed topology is studied by connecting the individual single topology in star connection in order to supply for different types load. We projected the results of following load

R-load (with and without filter)

Non-Linear load (with and without filter)

Induction Motor load

Fig.8 shows the simplified Circuit diagram of proposed Multi level inverter topology with Distributed PV power Generation System. The Switching pulses for IGBT's are generated by the same principle but the only difference is the Reference Waveform is phase shifted 120^0 for each phase in order to achieve Three Phase voltage at output. The equation for reference waveform is given as. (where m=modulation Index)

$V_{refa}=m*\sin(wt+0^0)$ Eq (1)

$V_{refb}=m*\sin(wt+120^0)$ Eq (2)

$V_{refc}=m*\sin(wt-120^0)$ Eq (3)

These loads are also tested with battery source as well as with a Renewable energy source (Photo voltaic cell).At first the basic output voltage from the three phase VSI system having the proposed topology and battery as DC source, is projected in Fig.8 a. The presence of 17^{th} order harmonics in the waveform in order to eliminate it we are coupling a LCL filter along across the load terminal. It can be designed from the relation of

$$f_0 = \frac{1}{\sqrt{LC}} \qquad Eq(4)$$

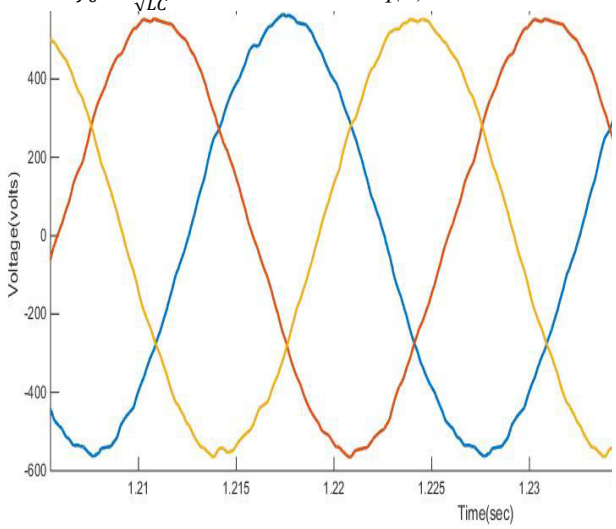


Fig9a. Output voltage waveform of proposed topology after Filter(R-Load)

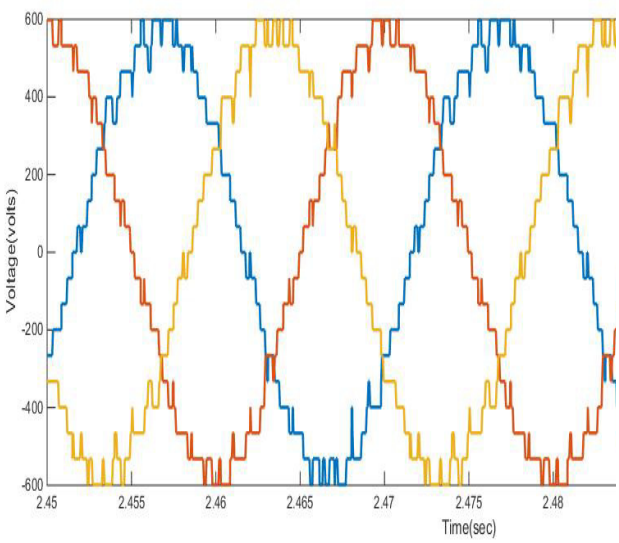


Fig8 a. Output voltage waveform of proposed system at three phase setup(R-Load)

After the coupling the output voltage will be looks exactly like a sinusoidal waveform which is projected at Fig.9a. And in current consumed by the load is also projected in Fig.9b.The FFT window at Fig.10 shows the mark able reduction in harmonics content of the waveform. The LCL filter not only attenuate the 17^{th} order harmonic but also the adjacent orders harmonics too due to roll off of the gain.

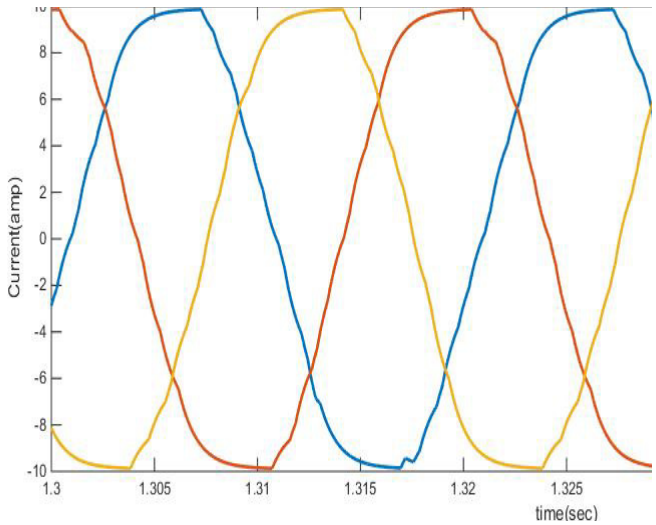


Fig9b. Output Current waveform of proposed topology after Filter(R-Load)

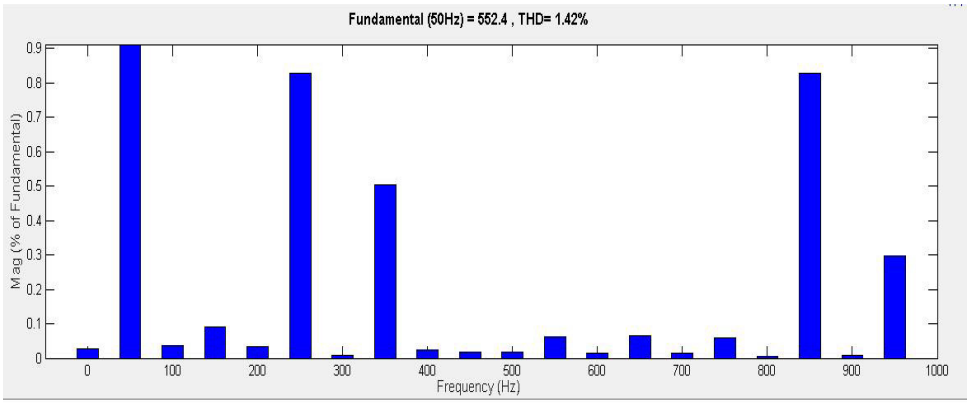


Fig10. FFT Window of output voltage with filter

C. Performance of proposed system at different Applications

For this performance analysis we preferred the Solar Inverter application. So an entire PV array is act as a DC source for proposed topology. On the other hands we prefer the standalone operation 3-phase induction motor and a nonlinear load (diode rectifier with RL-Load). We designed a PV array of rating 1580W with standard design of Voltage rating 24V and the performance of this individual array at different environmental conditions is projected at Fig.11a,b,c,d. It is the V-I and P-V characteristics of the designed individual PV module.

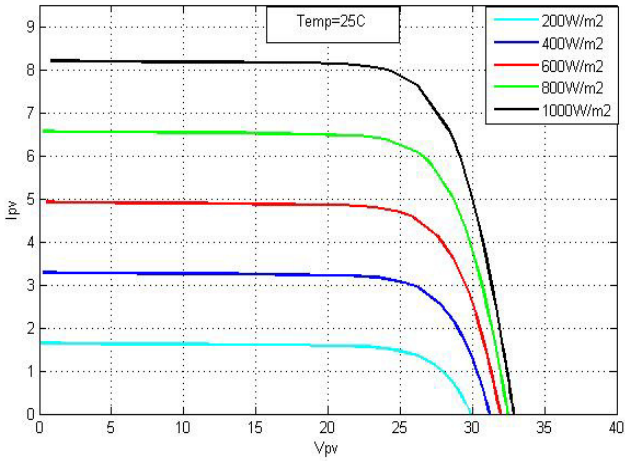


Fig11a.V-I characteristics at constant temperature

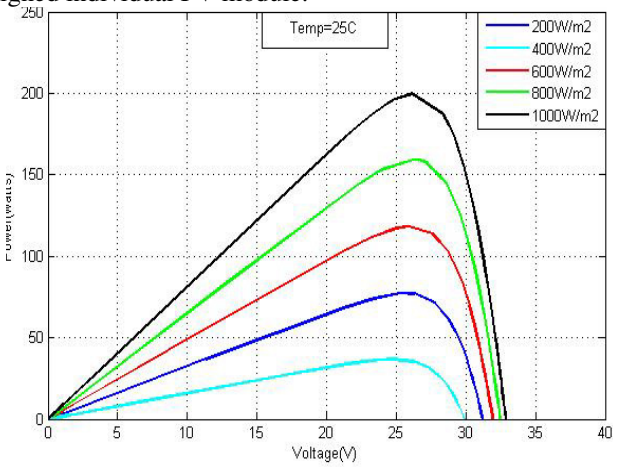


Fig11c.P-V characteristics at constant Temperature

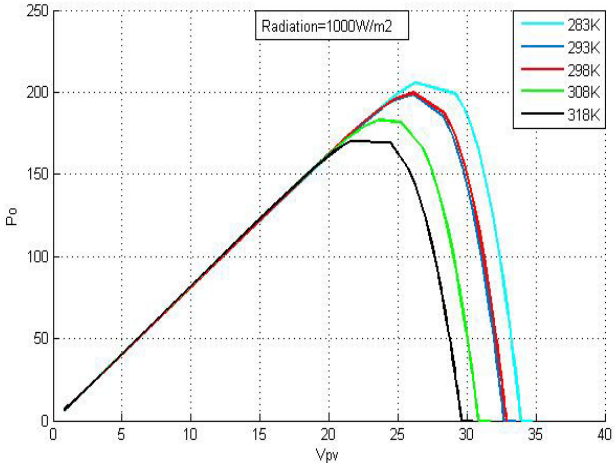


Fig11b.P-V characteristics at constant temperature

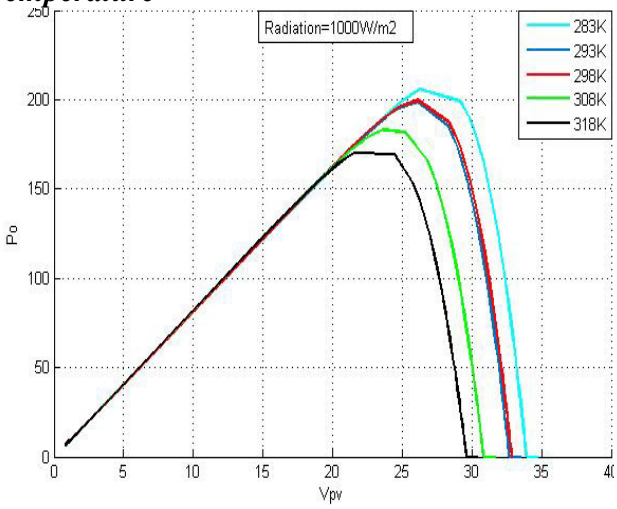


Fig11d.P-V characteristics at constant Radiation

The above designed PV panels are interconnected together to form a 20kW and 66.5V PV array. So these arrays are connected to real time loads like nonlinear load and Induction Motor Load. Here we simulated 15kw 600V nonlinear load, and 5HP IM as a real time load. The reason behind selecting these loads is, these ratings are mostly used for traction application.

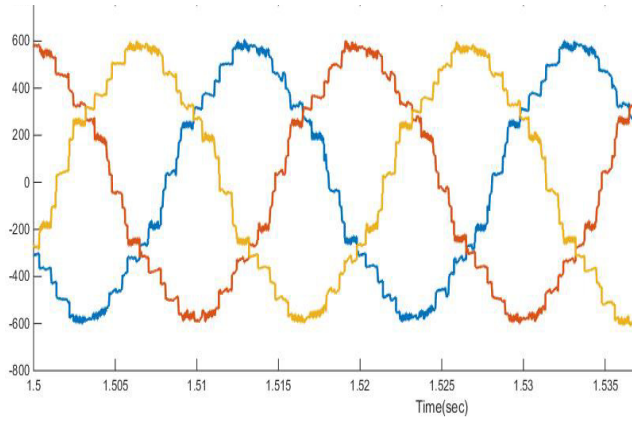


Fig12. Output voltage waveform of proposed system at three phase setup(Non Linear-Load)

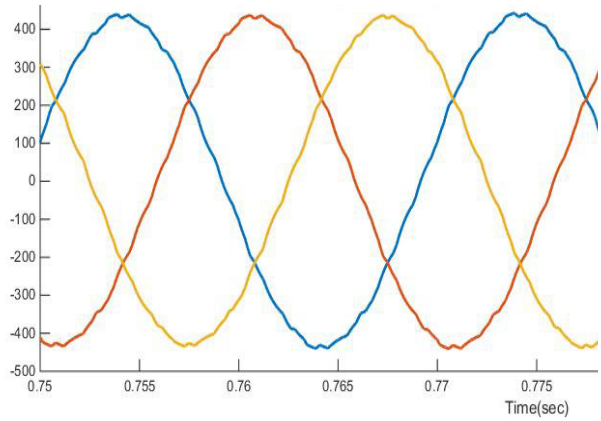


Fig13. Output voltage waveform of proposed system at three phase setup(Non Linear-Load)

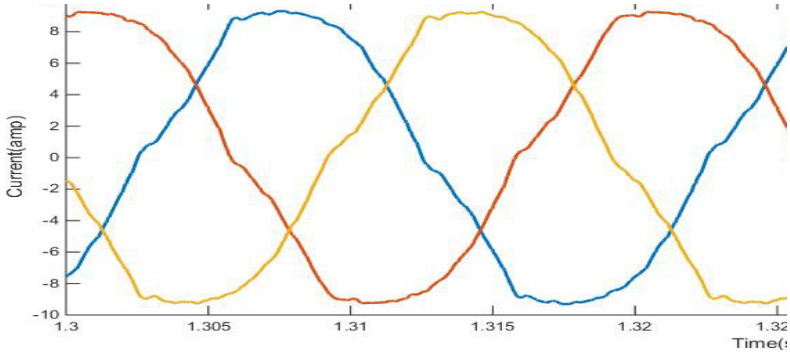


Fig14. Current Supplied to the Load with Filter (Non Linear-Load)

The Fig.12 shows the output voltage waveform of the proposed inverter loaded with a nonlinear load. There is no change or distortion is there in output voltage after replacing Battery input with renewable energy source. This is inferred from the above projected Waveform. But due to the presence of pure inductive filter the shape of voltage waveform get distorted which is projected in next plot Fig.13.But due to the presence of capacitive filter this effect get cancelled and the waveform looks exactly like sine wave.

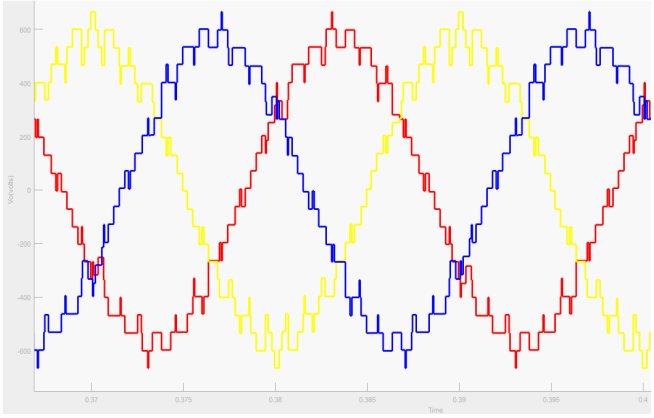
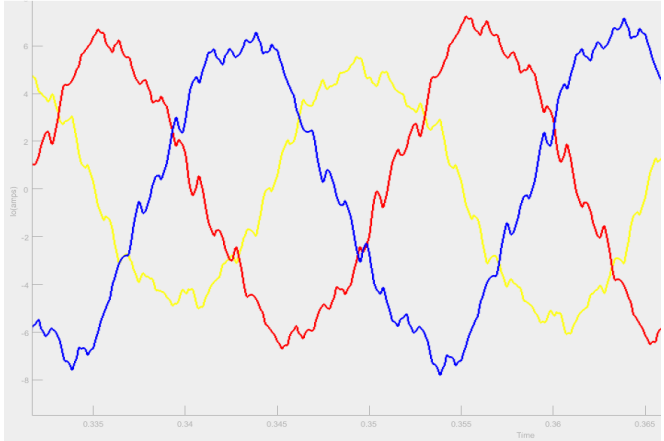


Fig13a. Output voltage waveform of proposed system at three phase setup(Motor Load)



.Fig13b. Output Current waveform of proposed system at three phase setup(Motor Load)

The Fig.13a shows the output voltage waveform of the proposed inverter loaded with a motor load. There is no change or distortion is there in output voltage after replacing Battery input with renewable energy source. This is inferred from the above projected Waveform. But due to the presence of capacitive filter the waveform looks exactly like sine wave which is projected in Fig 13b.

D. Result Comparison

Modulation Index	Maximum Output Voltage V_{om}	THD %	Maximum Output Voltage (after filter)	THD %	Real Power (Watts)	Reactive Power (Watts)
0.2	114.9	43.23	110.7	1.60	255	157
0.4	230	21.56	221.4	1.60	1100	610
0.6	345.4	15.92	332.7	1.59	2420	1400
0.8	457.5	8.98	440.5	1.56	4300	2500
1.0	573.6	8.5	552.4	1.42	6800	3900
1.2	622.1	8.24	599.2	1.45	8000	4600
1.4	633.5	5.66	639	1.56	9050	5200
1.6	676.4	6.17	651	1.67	9450	5230
1.8	685.6	6.2	660.3	1.65	9675	5600
2.0	694.1	6.66	668.4	1.68	9900	5700

Tab.2 Result analysis for R-Load

Modulation Index	Maximum Output Voltage V_{om}	THD %	Maximum Output Voltage (after filter)	THD %	Real Power (Watts)	Reactive Power (Watts)
0.2	114.1	43.23	109.4	3.63	425	325
0.4	224.8	21.94	216	3.37	1700	1300
0.6	345.2	15.77	332.7	3.84	3750	3000
0.8	459.4	9.31	440.5	3.55	6750	5250
1.0	559.4	11.13	552.4	3.40	9500	7500
1.2	629.3	9.62	599.2	3.40	13000	9750
1.4	670	6.62	639	3.39	14500	11200
1.6	684.9	6.82	651	3.38	15500	11750
1.8	694.9	6.11	660.3	3.38	16000	12000
2.0	708.4	6.01	668.4	3.39	16750	12250

Tab.3 Result analysis for Nonlinear Load

E. Hardware Results:

The Hardware setup for proposed multilevel inverter is tested with two 30V DC Sources in Lab environment. As mentioned above the multilevel gives 2n+1 (n, number of DC sources) level in the output voltage waveform which is shown in Fig 14b. The lab hardware setup is shown in Fig 14a.

Hardware Description:

i. Multi Tapping Transformer:

It is special type step down transformer which converts 230V/5*15V supply. It is used to supply the gate driving voltage required by the MOSFet/IGBT. Here for testing purpose we used Mosfet (IRF740) instead of IGBT. So we need a 15V DC gate driving supply.

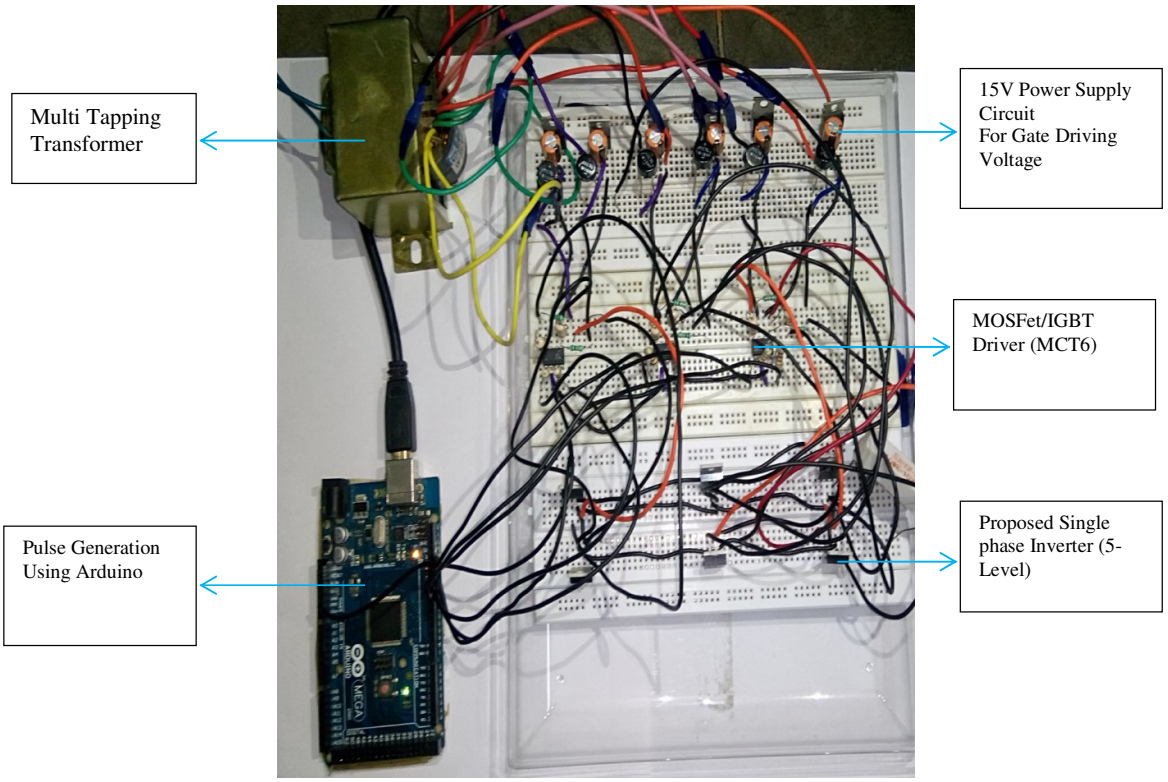
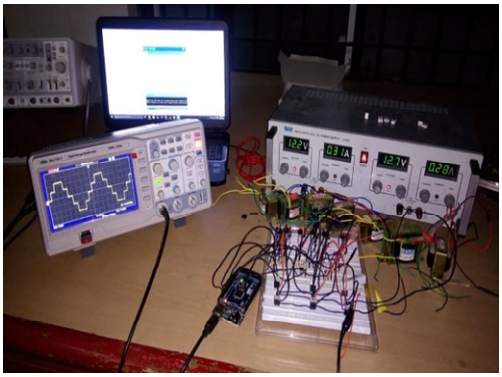
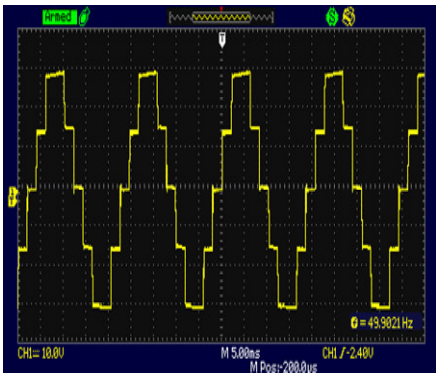


Fig14a.Hardware Prototype of proposed 5-Level Inverter



Five –level proposed MLI prototype



DSO output

Fig14b.Hardware Prototype of proposed 5-Level Inverter with Output

ii. Pulse Generation:

Here for pulse Generation we used Arduino mega2560. Here we used fixed pulse generation system for 5-level

iii. Gate Driver:

The gate driver for IRF740 is shown in Fig 14c which is used to strengthen the weak pulse signal from Ardiuno, as sufficient signal to drive a power MosFet.

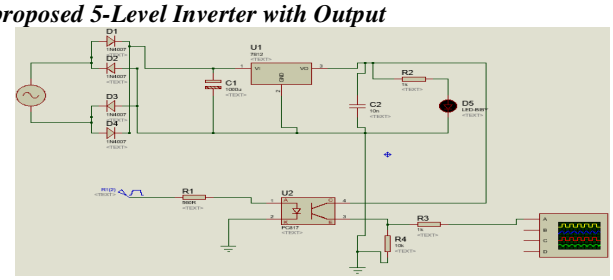


Fig14c. Opto-coupler Based MosFet Driver Circuit

IV. CONCLUSION

These paper proposed a topology in the field of Multilevel inverters to reduce power switches and the maximum count of component. It consists of individual floating dc sources connected in serious with other sources for the purpose of synthesizing of multilevel output waveform. The total harmonic distortion is reduced in the eleven level multilevel inverter of about **13.58%**. The main application of this paper is for Distributed Solar Power System. Its plays a major role integration n number of isolated solar plant into single grid. Simulation studies are done for the Eleven level inverter based on the proposed topology. The exploit and analysis of single phase Eleven level multilevel inverter are inquired by using an MATLAB/SIMULINK environment. Hardware test prototype is also constructed for 5 levels. Its Outputs are also validated with standard test cases.

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